Imperial College London

DE 1.3 – Electronics 1

Lecture 18 – 2017 Past Exam Paper

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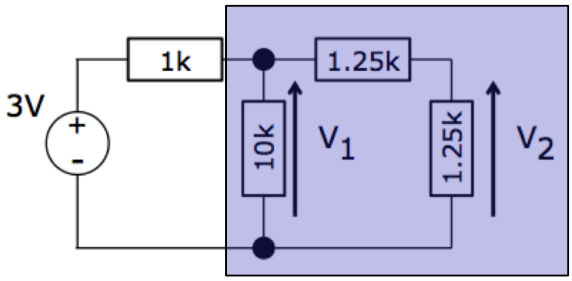
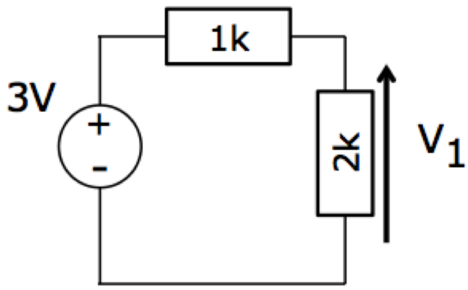
Q1 - voltage divider circuits (79%)

1. Find the value of V_1 and V_2 for the circuit shown in *Figure 1*. [10]



Find equivalent resistance of 10k // (1.25k+1.25k) = 2



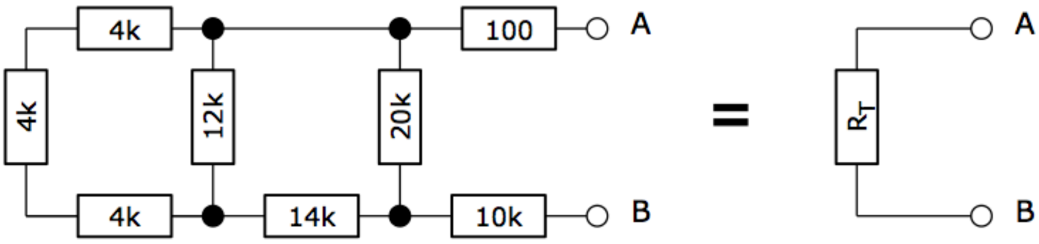
V1 is found by considering 2k and 1k as simple voltage divider. This gives V1 = 2V.

V2 is voltage divider of V1 by two 1.25k resistor. Therefore V2 = 1V

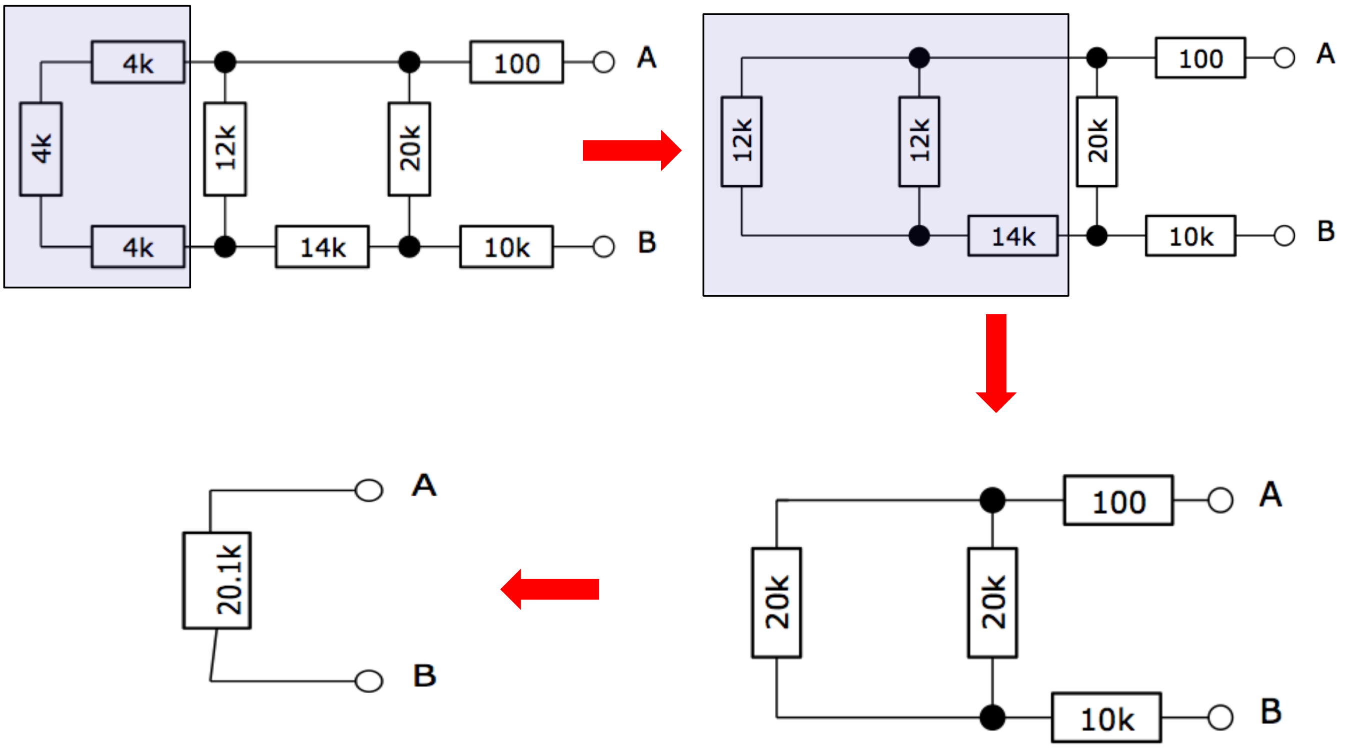
Q2 - Resistor network & Equivalent resistor

2. For the circuit shown in *Figure 2*, derive the equivalent resistance R_T between nodes A and B.

[10]



Q2 - Resistor network & Equivalent resistor (89%)



Q3 – Thévenin Equivalent Circuit

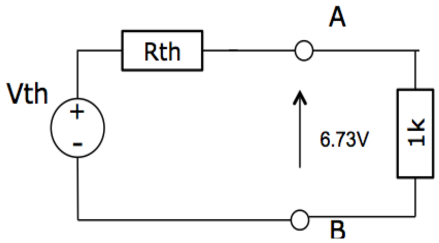
3. An electronic circuit with two terminals A and B is known to contain a battery and a network of resistors. The voltage between A and B is measured to be 6.73V when a 1kΩ resistor is connected between the two terminals. The voltage drops to 6.17V when the resistor is reduced to 200Ω.

   Derive the Thévinen equivalent circuit for the electronic circuit.

[10]

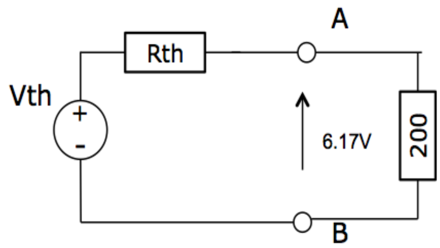
Q3 – Thévenin Equivalent Circuit (68%)

3. An electronic circuit with two terminals A and B is known to contain a battery and a network of resistors. The voltage between A and B is measured to be 6.73V when a 1kΩ resistor is connected between the two terminals. The voltage drops to 6.17V when the resistor is reduced to 200Ω.



This gives Eq 1:

$$6.73 = \frac{1}{1 + R_{th}} V_{th} \Rightarrow 6.73 + 6.73 R_{th} = Vth$$



This gives Eq 2:

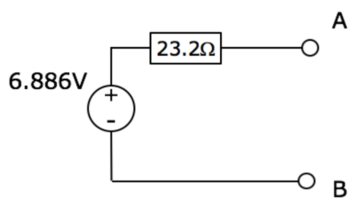
$$6.17 = \frac{0.2}{0.2 + R_{th}} V_{th} \Rightarrow 1.234 + 6.17 R_{th} = 0.2\, Vth$$

$$\Rightarrow 6.17 + 30.85\, R_{th} = Vth$$

Eq 1 – Eq 2 = 0.55

$$0.56 = 24.12\, R_{th}$$

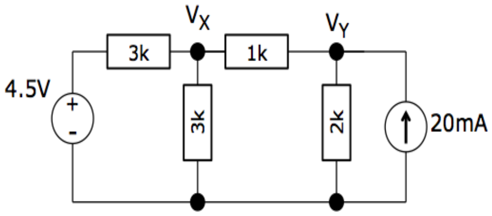
$$\Rightarrow R_{th} = 0.0232 \text{ or } 23.2\Omega.$$



Therefore Vth = 6.17 + 30.85 x 0.0232 = 6.886V.

Q4 - Principle of superposition (82%)

4. The circuit shown in *Figure 4* has a 4.5V voltage source and a 20mA current source. Using the method of nodal analysis, find the value of V_X and V_Y.



Apply KCL at node X:

$$\frac{X-4.5}{3}+\frac{X}{3}+\frac{X-Y}{1}=0$$
$$\Rightarrow 5X-3Y=4.5$$

Apply KCL at node Y:

$$\frac{Y-X}{1}+\frac{Y}{2}-20=0$$
$$\Rightarrow -2X+3Y=40$$

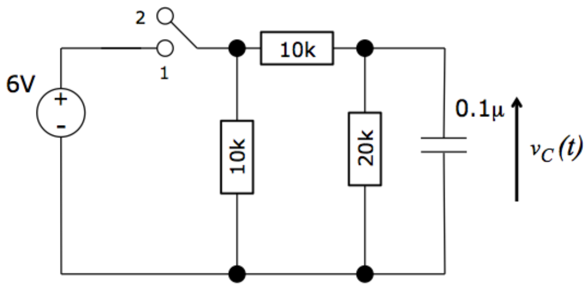
Therefore, 3X = 44.5, or X = 14.83V
Y = 23.2V

Q5 a & b – Transient behaviour of RC circuit

5. In the circuit shown in *Figure 5*, the switch is at position 2 (i.e. opened) for a long time before moving to position 1 (i.e. closed) at time t = 0 sec.

(a) What is the capacitor voltage $v_C(t)$ at t = 0 sec just before the switch is closed?

(b) What is the final value of v_C for $t \rightarrow \infty$?



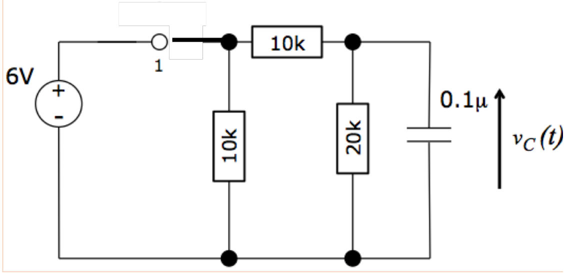
(a) Switch in position 2 means that the circuit was NOT connected to the voltage source. $v_C(0)$ = 0.

(b) When switch is closed, capacitor will charge up to value across 20k resistor as voltage divider. Therefore $v_C(\infty)$ = (20/(10+20)) x 6V = 4V.

Q5 c & d – Transient behaviour of RC circuit (50%)

(c) What is the time constant of the function $v_C(t)$ for $t \geq 0$ sec?

(d) Derive the equation for v_C as a function of time t.



(c) Equivalent resistance seen by capacitor when switch is closed is:

10k // 20k = 6.67k .

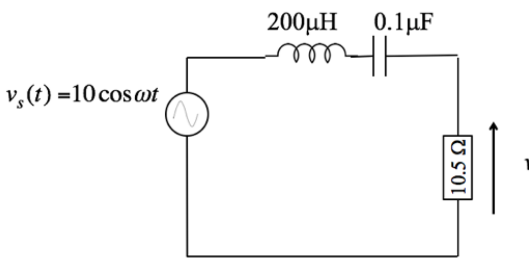
Therefore time constant = RC = 6.67 x 10^3 x 0.1 x 10^{-6} = 6.67 x 10^{-4}.

(d) $$V_c(t) = 4(1 - e^{-1.5\times10^3 t})$$

Q6 – Complex impedances

6. *Figure 6* shows a RLC circuit driven by a sinusoidal voltage source V_S with amplitude of 10V and a frequency of ω.

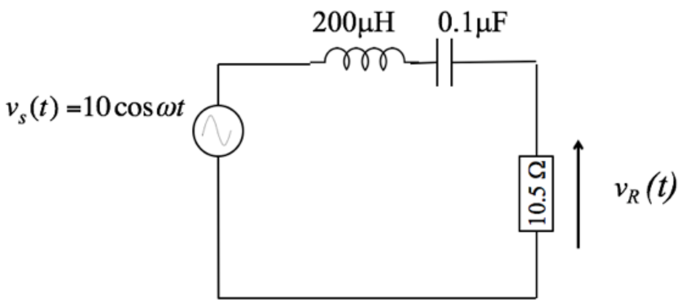
(i) Derive the complex impedance of the combined RLC circuit as a function of ω.



(i) $$Z = R + j\omega L + \frac{1}{j\omega C} = 10.5 + j(0.2\times10^{-3}\omega - \frac{10^7}{\omega})$$

Q6 – Complex impedances (47%)

(ii) Hence, or otherwise, derive the amplitude of the signal $V_R(t)$ across the resistor at DC and at signal frequency of 40 kHz.



(ii) Use voltage divider formula,

$$|V_R| = 10 \times \frac{10.5}{|Z|}$$

at 40kHz, $\omega = 251327$ rad/sec

Therefore

$|Z| = |10.5 + j(50.3 - 39.8)| = |10.5 + j10.5| = 14.95.$

Therefore, $|V_R| = 10 \times \frac{10.5}{|Z|} = 7.07V$

Q7 – Digital number representation (83%)

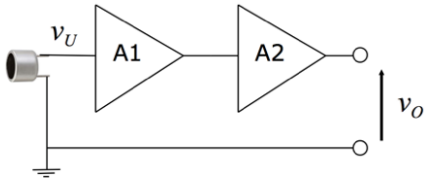
7. Given that the decimal code for the ASCII character 'A' is 65, and assuming that all numbers are represented using 8 bits, complete the missing entries that are not shaded in the following table (*Figure 7*). (No marks will be awarded for this question unless you show how the solutions are derived.)

Hexadecimal	Binary	Unsigned Decimal	ASCII
4C			
		165	

Hexadecimal	Binary	Unsigned Decimal	ASCII
4C	**01001100**	**76**	**'L'**
A5	**10100101**	165	

Q8 – Operational Amplifier (i)

8. *Figure 8a* shows a two-stage amplification system that detects the presence or absence of a 20kHz ultrasonic signal through the ultrasound senor. The range of the sensor signal V_U is 20mV peak-to-peak. The required output signal V_O is 4V peak-to-peak.
   (i) Using a single supply dual operational amplifier integrated circuit with a Gain-Bandwidth Product of 800kHz, determine with justification the gain values for the two-stage of amplification.



(i) Total gain require = 4V / 20mV = 200.

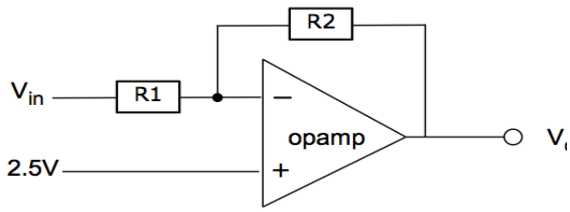
Since GBP = 800,000, the maximum gain at 20kHz would be 40.

Therefore, make A1 = 20, and A2 = 10 would work well.

Q8 – Operational Amplifier (ii)

(ii) *Figure 8b* shows the circuit for stage 2 of the amplification system. Assuming that the operational amplifier uses a +5V supply and is able to provide rail-to-rail output. Prove that the gain of this amplifier is given by:

$$V_{out} = -\frac{R2}{R1}(V_{in} - 2.5) + 2.5$$



The circuit works like this. Voltage at –ve input is 2.5V. Apply KCL at this node give:

$$\frac{V_{out} - 2.5}{R2} = \frac{-(V_{in} - 2.5)}{R1}$$

$$\Rightarrow V_{out} = -\frac{R2}{R1}(V_{in} - 2.5) + 2.5$$

Q8 – Operational Amplifier (iii) (54%)

(iii) Hence or otherwise, design the circuit for your answer to Question 8 (i).

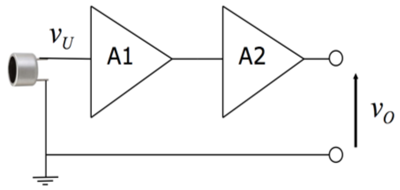


Figure 8a

If A2 = 10, one solution is R2 = 100k, R1 = 10k.

Q9 – PWM and motor speed control (i)

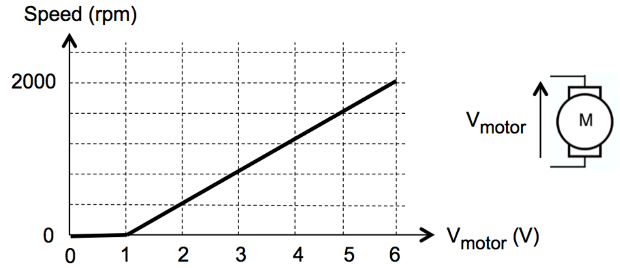
9. *Figure 9* shows the relationship between the speed of a DC motor (in revolutions per minute or rpm) and the average voltage across the motor windings.

   (i) Explain the advantage of controlling the speed of a DC motor with a pulse-width modulation (PWM) signal instead of a DC voltage.

Q9 – PWM and motor speed control (ii) (48%)

9. *Figure 9* shows the relationship between the speed of a DC motor (in revolutions per minute or rpm) and the average voltage across the motor windings.

(ii) A robot car uses four DC motors with a no-load speed vs drive voltage curve as shown in *Figure 9*. The wheels of the car have a diameter of 6 cm. What is the duty-cycle of the driving PWM signal if the car is to travel at a speed of 5m/sec? State any assumption used.



6cm wheel provides 18.85cm/rev.

Therefore 5m/sec speed requires 5/0.1885 = 26.52 rev/sec = 1591 rpm.

Therefore Vmotor = 5V x 1591/2000 + 1V = 4.98V.
Hence,
Duty cycle = 4.98/6 = 83%.